REMARKS

Claims 1, 3, 6, 14-15, 29, 31-34, 36 and 41-46 have been amended. Claim 1 and new claims 53-58 correspond to elected claims. Claims 3-12, 14-18, 20-21, 28-29, 31-34, and 36-50 are been withdrawn from consideration as non-elected claims, but have been amended so that they depend, directly or indirectly, upon elected claims. Claims 2, 13, 19, 22-27, 30, 35, and 51-52 have been canceled. Claims 1, 3-12, 14-18, 20-21, 28-29, 31-34, and 36-50 and 53-58 are pending in the present application.

Initially, applicant points out that claim 1 is generic to claims 3-12, 14-18, 20-21, 28-29, 31-34, and 36-50. Accordingly, even though these claims have been withdrawn from consideration as non-elected claims, if claim 1 is determined to be allowable, these claims should also be allowed.

Claims 1-2 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Asnaashari (U.S. Patent No. 6,076,137). Claims 1-2 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Day (U.S. Patent No. 6,065,096) in view of Bolt (U.S. Patent No. 6,467,014). Claim 2 has been canceled. These rejections, to the extent that they apply to claim 1 and new claims 53-58 are respectfully traversed.

Claim 1 recites, *inter alia*, "An integrated input/output controller integrated into a single integrated circuit device, comprising: a host interface subsystem ...including a command decode controller for parsing host commands to identify data flow type host commands and non data flow type commands ... wherein for each data flow type host command, said command decode controller communicates an associated logical block address to the mapping controller, said mapping controller converts the associated logical block address to an associated peripheral block address, and said peripheral interface subsystem accesses the one or more peripherals using said associated peripheral block address."

Claims 56 recites, *inter alia*, "A[n] ... controller integrated into a single integrated circuit device, comprising: a microcontroller subsystem for processing non data flow type host commands; and a data flow subsystem for processing data flow type host commands, said data flow subsystem comprising, ... a cache manager subsystem for managing a cache memory, said cache manager subsystem receiving the cache manager packet, if data associated with said cache manager packet is stored in the cache memory, forwarding read data from the cache to the host exchange controller if the host command is a read command, accepting write data from the host exchange controller if the host command is a write command, and, if data associated with said cache manager packet is not stored in the cache memory, forwarding a logical block address associated with said cache manager packet to the mapping controller to receive an associated peripheral block address, said peripheral interface subsystem accessing at least one peripheral using said associated peripheral block address."

Asnaashari is directed to a controller for a flash memory system. Asannashari's controller performs a mapping between logical block addresses and physical block addresses for flash memory devices, through the use of a primary buffer and a secondary buffer. The controller of Asannashari is capable of swapping the roles of the primary and secondary buffers as necessary.

Amended claim 1 and new claim 56 recite a command decode controller which parses host commands to identify the host command as being either a data flow type host command or a non data flow type command. This is important because only data flow type host commands, and not non data flow type commands, are processed by the mapping controller to map the logical block addresses into peripheral block addresses. Specifically, non data flow type host commands are processed directly by a microcontroller circuit (see claim 14). Asnaashari is devoid of any teaching or suggestion regarding parsing host commands to identify the commands as data flow

types commands or non data flow commands. Accordingly, Asnaashari fails to disclose or suggest the above quoted limitations of independent claims 1 and 56.

The Examiner also cites Day, which discloses a single chip RAID controller, and Bolt which discloses an address translator for multi-zone storage devices. However, these two references also fail to disclose or suggest parsing host commands to identify the commands as either data flow type commands or non data flow type commands. Accordingly, Day and Bolt, whether taken singly or in combination, fail to disclose or suggest the above quoted limitations of independent claims 1 and 56.

Additionally claim 56 further recite a specific architecture for the I/O controller of the present invention. More specifically, claim 56 include limitations directed to communications between several functional units of the present invention. The specific functional units recited, and the type of communication between the specific functional units, are not taught or suggested by the prior art of record.

Accordingly, claims 1 and 56 are believed to be allowable over the art of record. Dependent claims 53-55 and 57-58 are believed to be allowable for at least the same reasons as stated above with respect to the independent claims.

Applicant also points out that withdrawn claim 15 recites, *inter alia* ,"a cache manager coupled to the host interface subsystem and the peripheral interface subsystem, the cache manager to manage entries in a cache buffer to temporarily store data of the data flow between the peripheral and the host." Withdrawn claim 32 recites, *inter alia*, "the command decode controller maintains a command queue for each volume accessible by the at least one hosts to further validate a host command and to queue the host command for execution." These features are also not taught or suggested by the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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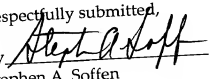
Respectfully submitted,

By 

Stephen A. Soffen
Registration No.: 31,063
Christopher S. Chow
Registration No.: 46,493
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant